What is claimed is:

1. A single charge trapping layer for storing electrical charge in a memory device comprising a high-k dielectric material.

2. A charge trapping layer as in claim 1 further subjected to a treatment process to improve the charge trapping characteristic.

3. A charge trapping layer as in claim 2 wherein the treatment process is a plasma exposure or an ion implantation exposure.

4. A charge trapping layer as in claim 3 wherein the plasma exposure comprises at least a plasma oxygen exposure, a plasma nitrogen exposure, or a plasma hydrogen exposure.

5. A charge trapping layer as in claim 3 wherein the plasma exposure time is between 10 seconds and 100 seconds.

6. A charge trapping layer as in claim 1 wherein the high-k dielectric material comprises at least one of aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), zirconium oxide (ZrO_2), titanium oxide (TiO_2), tantalum oxide (Ta_2O_5), cesium oxide (CeO_2), lanthanum oxide (La_2O_3), tungsten oxide (WO_3), yttrium oxide (Y_2O_3), bismuth silicon oxide ($Bi_4Si_2O_{12}$), barium strontium oxide ($Ba_{1-x}Sr_xO_3$), lanthanum aluminum oxide ($LaAlO_3$), hafnium silicate ($HfSiO_4$), zirconium silicate ($ZrSiO_4$), aluminum hafnium oxide (AlHfO), aluminum oxynitride (AlON), hafnium silicon oxynitride (HfSiON), zirconium silicon oxynitride (ZrSiON), barium titanate ($BaTiO_3$), strontium titanate ($SrTiO_3$), lead titanate ($PbTiO_3$), barium strontium titanate (BST) ($Ba_{1-x}Sr_xTiO_3$), lead zirconium titanate, lead lanthanum titanate, bismuth titanate, strontium titanate, lead zirconium titanate (PZT ($PbZr_xTi_{1-x}O_3$))

barium zirconium titanate, strontium bismuth tantalate, lead zirconate ($PbZrO_3$), PZN ($PbZn_xNb_{1-x}O_3$), PST ($PbSc_xTa_{1-x}O_3$), or PMN ($PbMg_xNb_{1-x}O3$).

7. A non-volatile memory transistor comprising:

source and drain regions provided in a substrate; and

a gate structure on the substrate between the source and drain regions, the gate structure comprising

a single charge trapping layer overlying the substrate, the charge trapping layer comprising a high-k dielectric material; and

an electrode layer overlying the charge trapping layer.

8. A memory transistor as in claim 7 wherein the high-k dielectric material comprises at least hafnium oxide (HfO_2).

9. A memory transistor as in claim 7 wherein the high-k dielectric material comprises at least one of aluminum oxide (Al_2O_3), zirconium oxide (ZrO_2), titanium oxide (TiO_2), tantalum oxide (Ta_2O_5), cesium oxide (CeO_2), lanthanum oxide (La_2O_3), tungsten oxide (WO_3), yttrium oxide (Y_2O_3), bismuth silicon oxide ($Bi_4Si_2O_{12}$), barium strontium oxide ($Ba_{1-x}Sr_xO_3$), lanthanum aluminum oxide ($LaAlO_3$), hafnium silicate ($HfSiO_4$), zirconium silicate ($ZrSiO_4$), aluminum hafnium oxide (AlHfO), aluminum oxynitride (AlON), hafnium silicon oxynitride (HfSiON), zirconium silicon oxynitride (ZrSiON), barium titanate ($BaTiO_3$), strontium titanate ($SrTiO_3$), lead titanate ($PbTiO_3$), barium strontium titanate (BST) ($Ba_{1-x}Sr_xTiO_3$), lead zirconium titanate, lead lanthanum titanate, bismuth titanate, strontium titanate, lead zirconium titanate (PZT ($PbZr_xTi_{1-x}O_3$)) barium zirconium titanate, strontium bismuth tantalate, lead zirconate ($PbZrO_3$), PZN ($PbZn_xNb_{1-x}O_3$), PST ($PbSc_xTa_{1-x}O_3$), or PMN ($PbMg_xNb_{1-x}O3$).

10. A memory transistor as in claim 7 wherein the charge trapping layer is subjected to a treatment process to improve the charge trapping characteristic.

11. A charge trapping layer as in claim 10 wherein the treatment process is a plasma exposure or an ion implantation exposure.

12. A charge trapping layer as in claim 11 wherein the plasma exposure comprises at least a plasma oxygen exposure, a plasma nitrogen exposure, or a plasma hydrogen exposure.

13. A charge trapping layer as in claim 11 wherein the plasma exposure time is between 10 seconds and 100 seconds.

14. A memory transistor as in claim 7 wherein the electrode layer is a layer of doped polysilicon, a layer of silicide, or a layer of metal.

15. A memory transistor as in claim 7 wherein the memory transistor is a multi-bit memory transistor.

16. A method of fabricating a non-volatile memory transistor comprising the steps of:

preparing a semiconductor substrate;

forming a gate stack on the substrate, the gate stack comprising

a single charge trapping layer overlying the substrate wherein the charge trapping layer comprises a high-k dielectric material; and

an electrode layer overlying the charge trapping layer; and

forming drain and source regions on opposite sides of the gate stack.

17. A method as in claim 16 wherein the high-k dielectric material comprises at least one of aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), zirconium

oxide (ZrO_2), titanium oxide (TiO_2), tantalum oxide (Ta_2O_5), cesium oxide (CeO_2), lanthanum oxide (La_2O_3), tungsten oxide (WO_3), yttrium oxide (Y_2O_3), bismuth silicon oxide ($Bi_4Si_2O_{12}$), barium strontium oxide ($Ba_{1-x}Sr_xO_3$), lanthanum aluminum oxide ($LaAlO_3$), hafnium silicate ($HfSiO_4$), zirconium silicate ($ZrSiO_4$), aluminum hafnium oxide (AlHfO), aluminum oxynitride (AlON), hafnium silicon oxynitride (HfSiON), zirconium silicon oxynitride (ZrSiON), barium titanate ($BaTiO_3$), strontium titanate ($SrTiO_3$), lead titanate ($PbTiO_3$), barium strontium titanate (BST) ($Ba_{1-x}Sr_xTiO_3$), lead zirconium titanate, lead lanthanum titanate, bismuth titanate, strontium titanate, lead zirconium titanate (PZT ($PbZr_xTi_{1-x}O_3$)) barium zirconium titanate, strontium bismuth tantalate, lead zirconate ($PbZrO_3$), PZN ($PbZn_xNb_{1-x}O_3$), PST ($PbSc_xTa_{1-x}O_3$), or PMN ($PbMg_xNb_{1-x}$O3).

18. A method as in claim 16 wherein the charge trapping layer is subjected to a treatment process to improve the charge trapping characteristic.

19. A method as in claim 18 wherein the treatment process is a plasma exposure or an ion implantation exposure.

20. A method as in claim 19 wherein the plasma exposure comprises at least a plasma oxygen exposure, a plasma nitrogen exposure, or a plasma hydrogen exposure.

21. A method as in claim 19 wherein the plasma exposure time is between 10 seconds and 100 seconds.

22. A method as in claim 16 wherein the charge trapping layer is deposited by ALD method.

23. A method as in claim 16 further comprising a densification anneal step after deposition of the charge trapping layer.

24. A method as in claim 16 wherein the formation of the drain and source regions comprises an angle source and drain implantation.

25. A method as in claim 16 wherein the semiconductor substrate is selected from a group consisted of SOI substrate, bulk silicon substrate, and insulator substrate.

26. A method as in claim 16 wherein the memory transistor is a multi-bit memory transistor.